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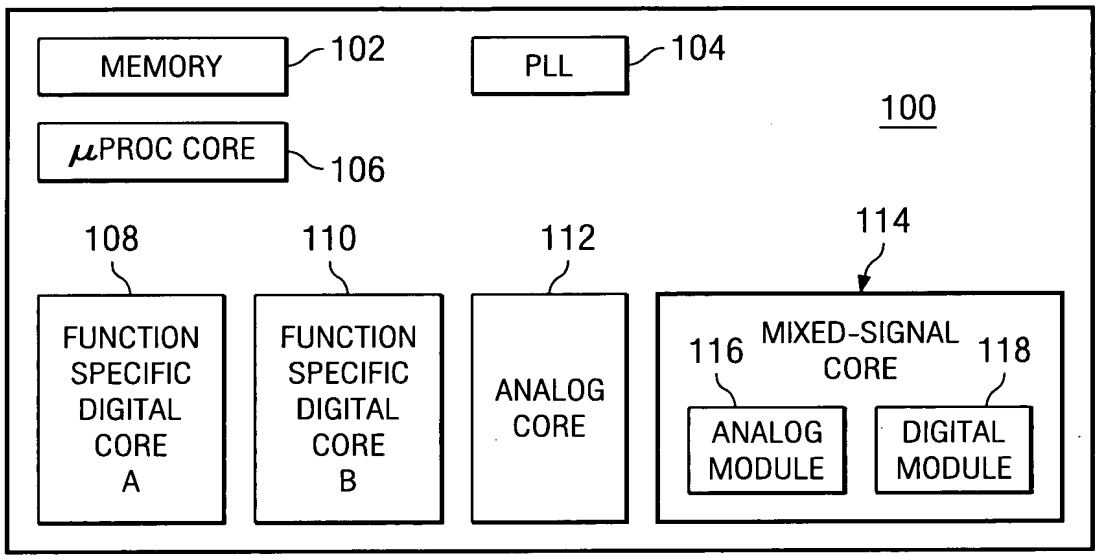

FIG. 1

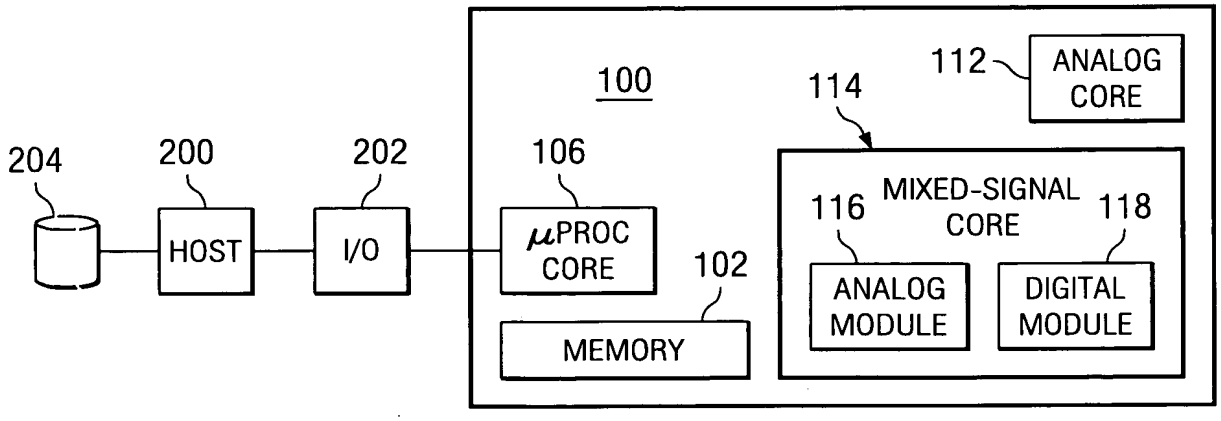

FIG. 2

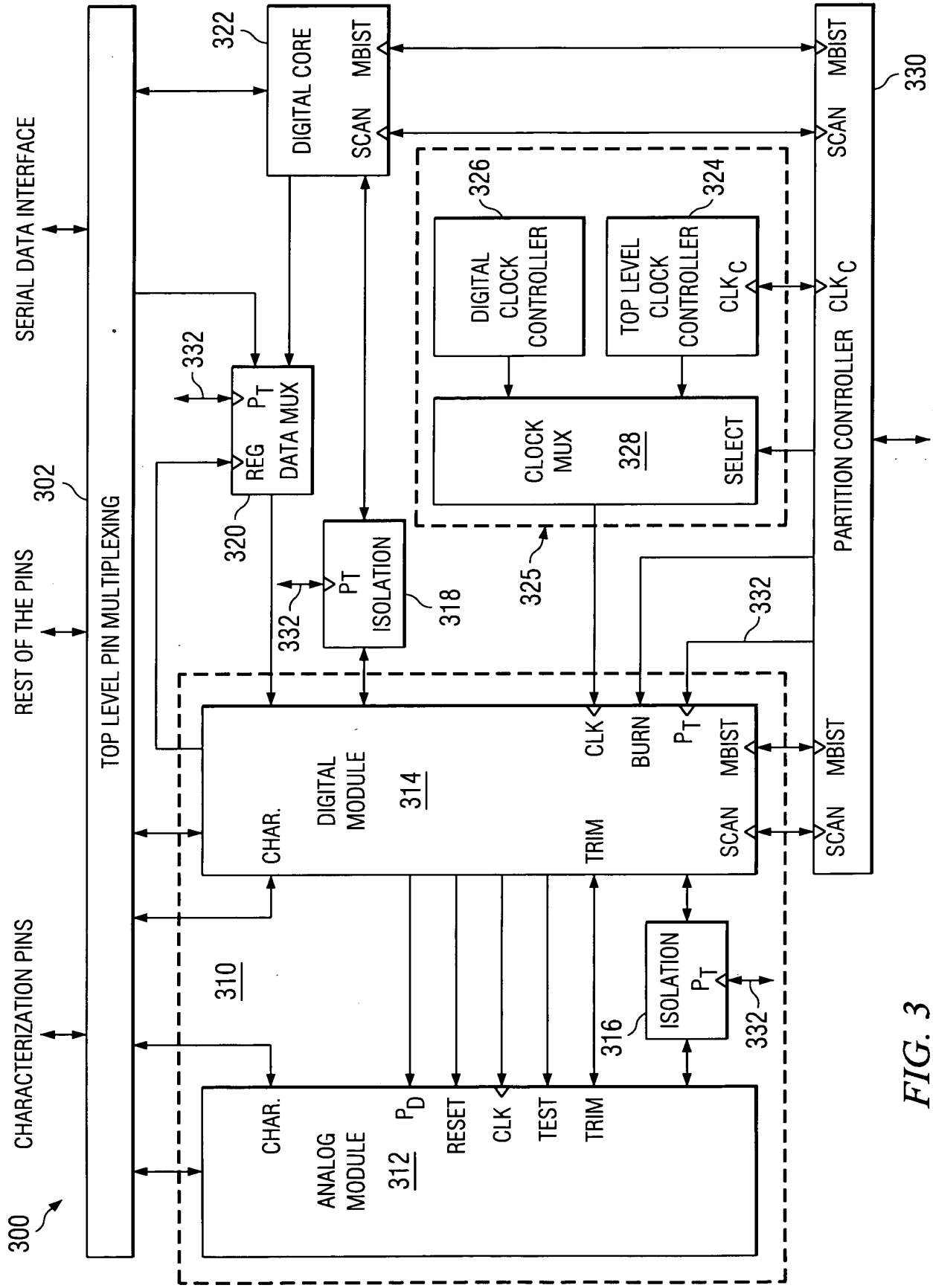
300
CHARACTERIZATION PINS
REST OF THE PINS
SERIAL DATA INTERFACE
302
TOP LEVEL PIN MULTIPLEXING
310
312
ANALOG MODULE
CHAR.
P_D
RESET
CLK
TEST
TRIM
314
DIGITAL MODULE
CHAR.
CLK
BURN
P_T
MBIST
SCAN
TRIM
316
ISOLATION P_T
318
PT ISOLATION
320
REG P_T DATA MUX
322
DIGITAL CORE
MBIST
SCAN
324
TOP LEVEL CLOCK CONTROLLER
CLK_C
326
DIGITAL CLOCK CONTROLLER
328
CLOCK MUX
SELECT
325
330
PARTITION CONTROLLER
CLK_C
MBIST
SCAN
TEST CLOCK AND TEST CONTROL PINS
332

FIG. 3

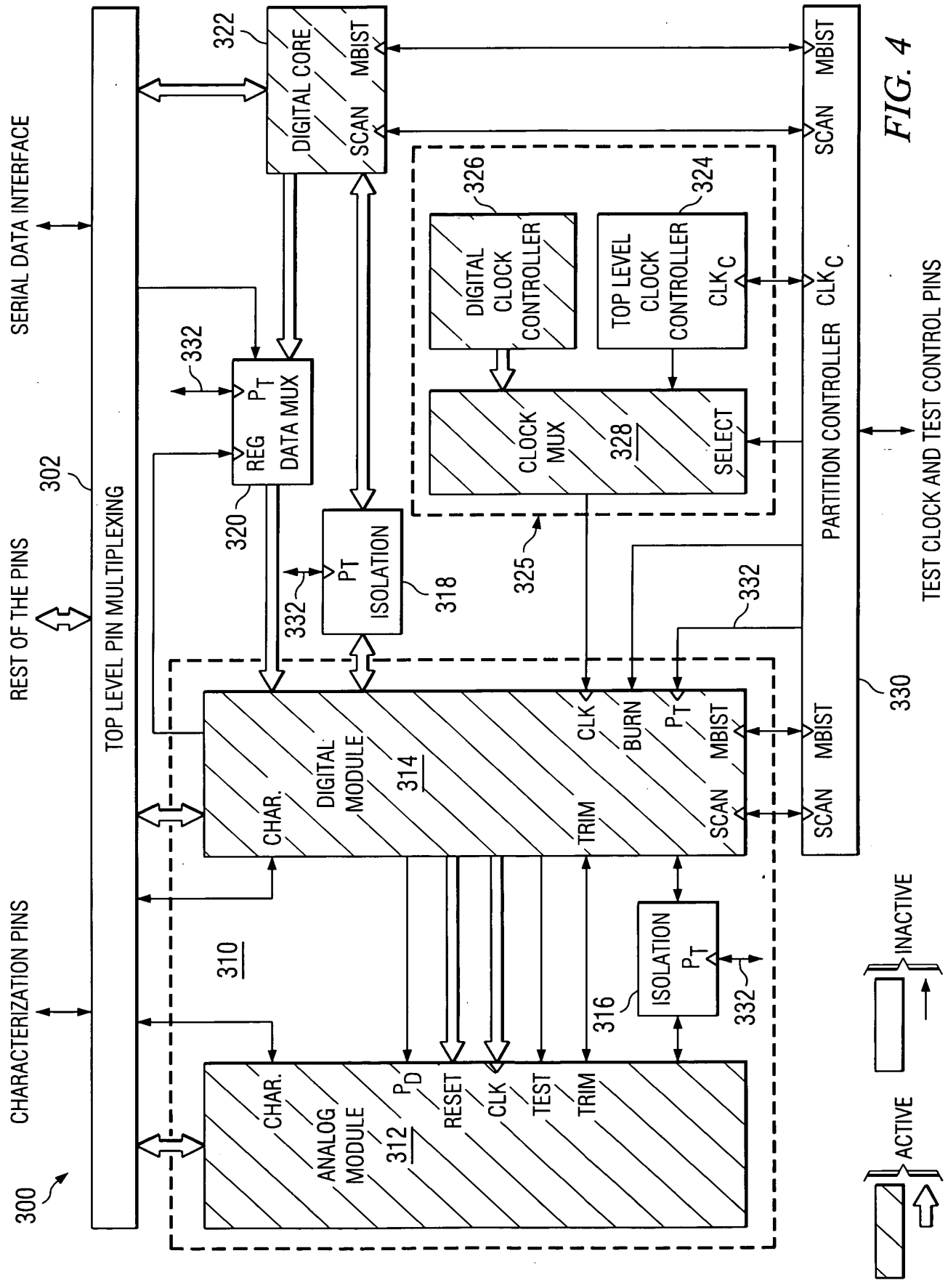
SERIAL DATA INTERFACE
REST OF THE PINS
CHARACTERIZATION PINS
TOP LEVEL PIN MULTIPLEXING
302
300
322
DIGITAL CORE
SCAN
MBIST
326
DIGITAL CLOCK CONTROLLER
324
TOP LEVEL CLOCK CONTROLLER
CLKC
332
PT
REG
DATA MUX
320
CLOCK MUX
328
SELECT
325
PT ISOLATION
318
PARTITION CONTROLLER
TEST CLOCK AND TEST CONTROL PINS
330
DIGITAL MODULE
314
CHAR.
TRIM
CLK
BURN
ISOLATION PT
316
310
ANALOG MODULE
312
PD
RESET
TEST
INACTIVE
ACTIVE

FIG. 4

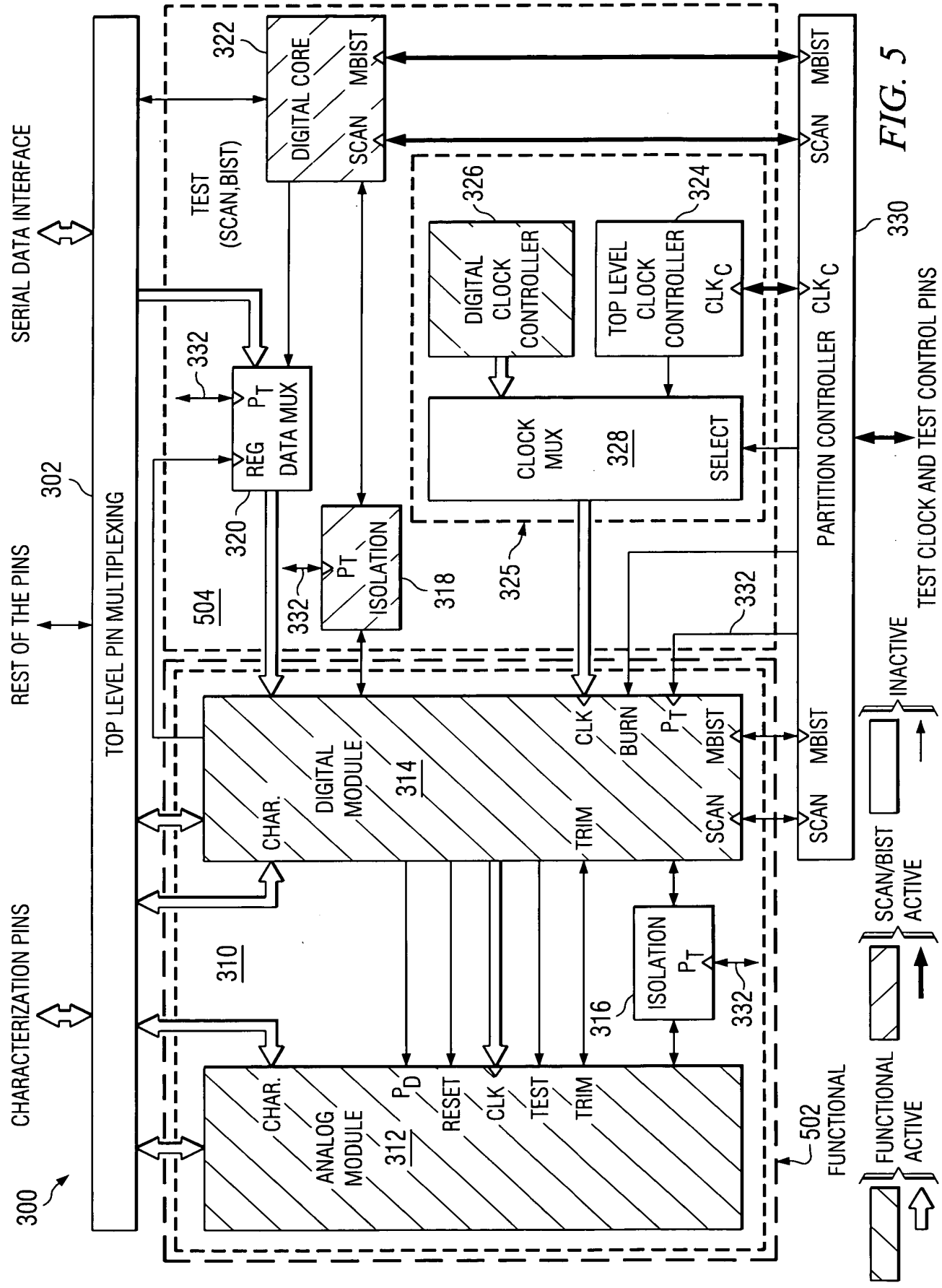
SERIAL DATA INTERFACE
REST OF THE PINS
CHARACTERIZATION PINS
300
302
TOP LEVEL PIN MULTIPLEXING
322
DIGITAL CORE
MBIST
SCAN
TEST (SCAN,BIST)
326
DIGITAL CLOCK CONTROLLER
324
TOP LEVEL CLOCK CONTROLLER
CLKC
330
PARTITION CONTROLLER
CLKC
SCAN
MBIST
332
REG
PT
DATA MUX
320
504
PT
ISOLATION
318
325
CLOCK MUX
328
SELECT
TEST CLOCK AND TEST CONTROL PINS
INACTIVE
SCAN/BIST ACTIVE
FUNCTIONAL ACTIVE
DIGITAL MODULE
314
CHAR.
CLK
BURN
PT
MBIST
SCAN
TRIM
310
316
ISOLATION
PT
ANALOG MODULE
312
CHAR.
PD
RESET
CLK
TEST
TRIM
502
FUNCTIONAL

FIG. 5

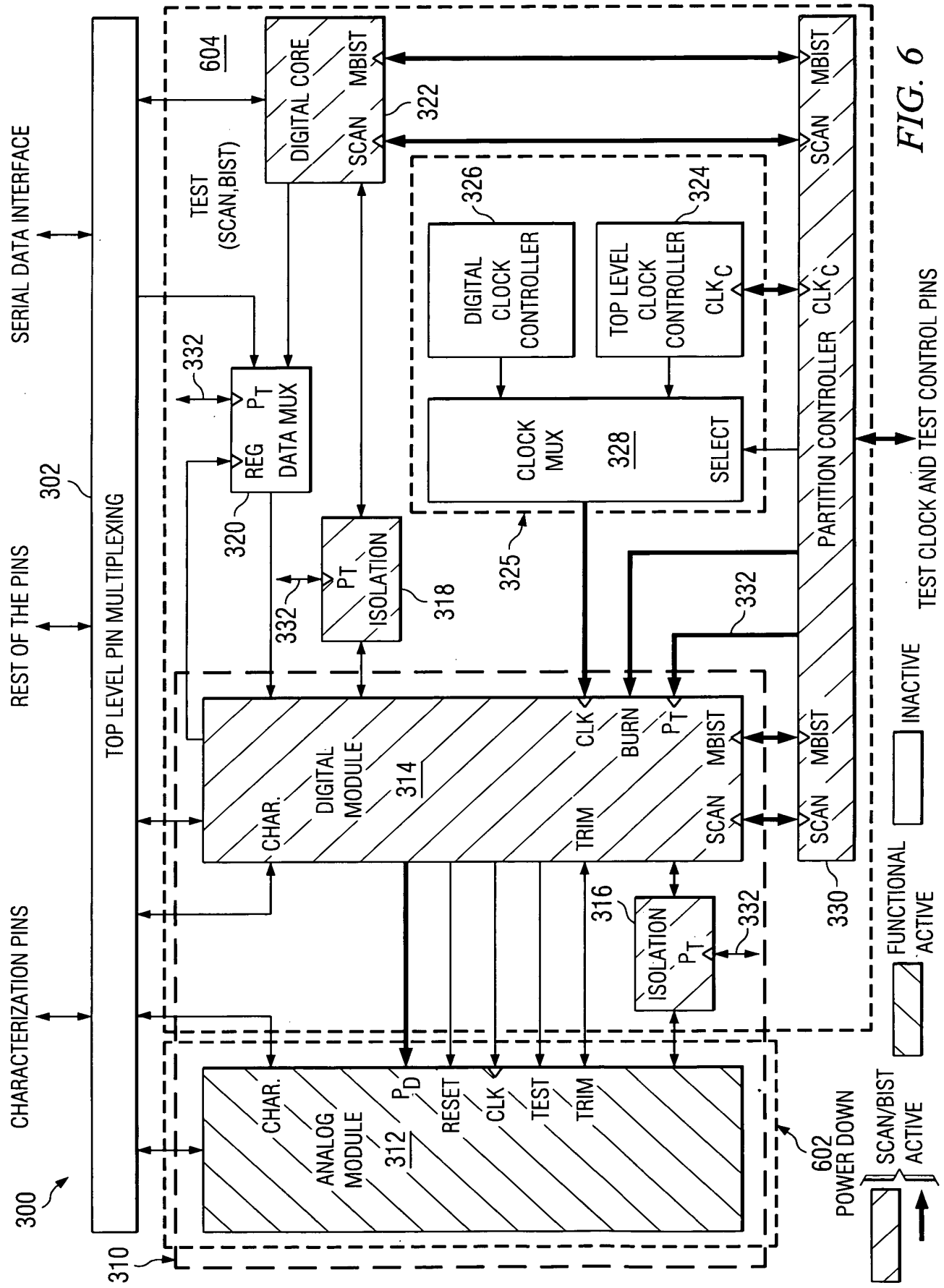
SERIAL DATA INTERFACE
REST OF THE PINS
CHARACTERIZATION PINS
TOP LEVEL PIN MULTIPLEXING
302
300
310
604
DIGITAL CORE
MBIST
SCAN
322
TEST (SCAN,BIST)
326
DIGITAL CLOCK CONTROLLER
324
TOP LEVEL CLOCK CONTROLLER
CLKC
CLOCK MUX
328
SELECT
325
332
REG
PT
DATA MUX
320
ISOLATION
318
DIGITAL MODULE
314
CHAR.
CLK
BURN
TRIM
316
ISOLATION
330
PARTITION CONTROLLER
TEST CLOCK AND TEST CONTROL PINS
ANALOG MODULE
312
PD
RESET
CLK
TEST
TRIM
602
POWER DOWN
INACTIVE
FUNCTIONAL ACTIVE
SCAN/BIST ACTIVE

FIG. 6